ABSTRACT:

Circuit configuration for generating the drive signal (HDRV) for the deflection transistor that drives the oscillating circuit for the horizontal deflection of a cathode ray tube (CRT). The circuit configuration in accordance with the invention generates a second, horizontal reference signal (HREF2), which, viewed over time, lies between the signal for the horizontal flyback (HFB) and the square-wave signal of the drive signal (HDRV) for the deflection transistor, for all possible horizontal positions (hpos) and horizontal modulations (hmod). Connected between the output of the first phase-lock loop (PLL1) and the input of the second phase-lock loop (PLL2) is a delay block (DB1). In accordance with the invention, the phase measurement of the horizontal flyback (HFB) in relation to the second horizontal reference signal (HREF2) always takes place in the time constituting 10% of a period. For the positioning of the second horizontal reference signal (HREF2), the first delay block (DB1) is, in accordance with the invention, added to the conventional circuit configuration.

Fig. 1a